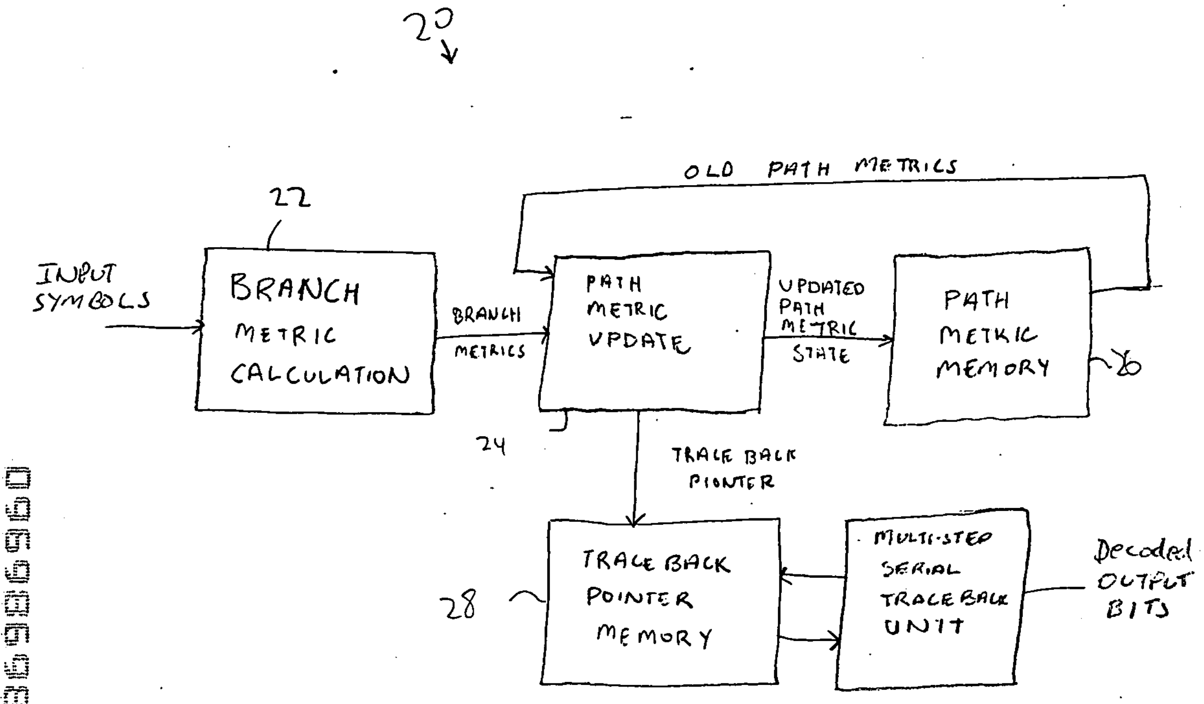


(CONVENTIONAL)

FIGURE 1

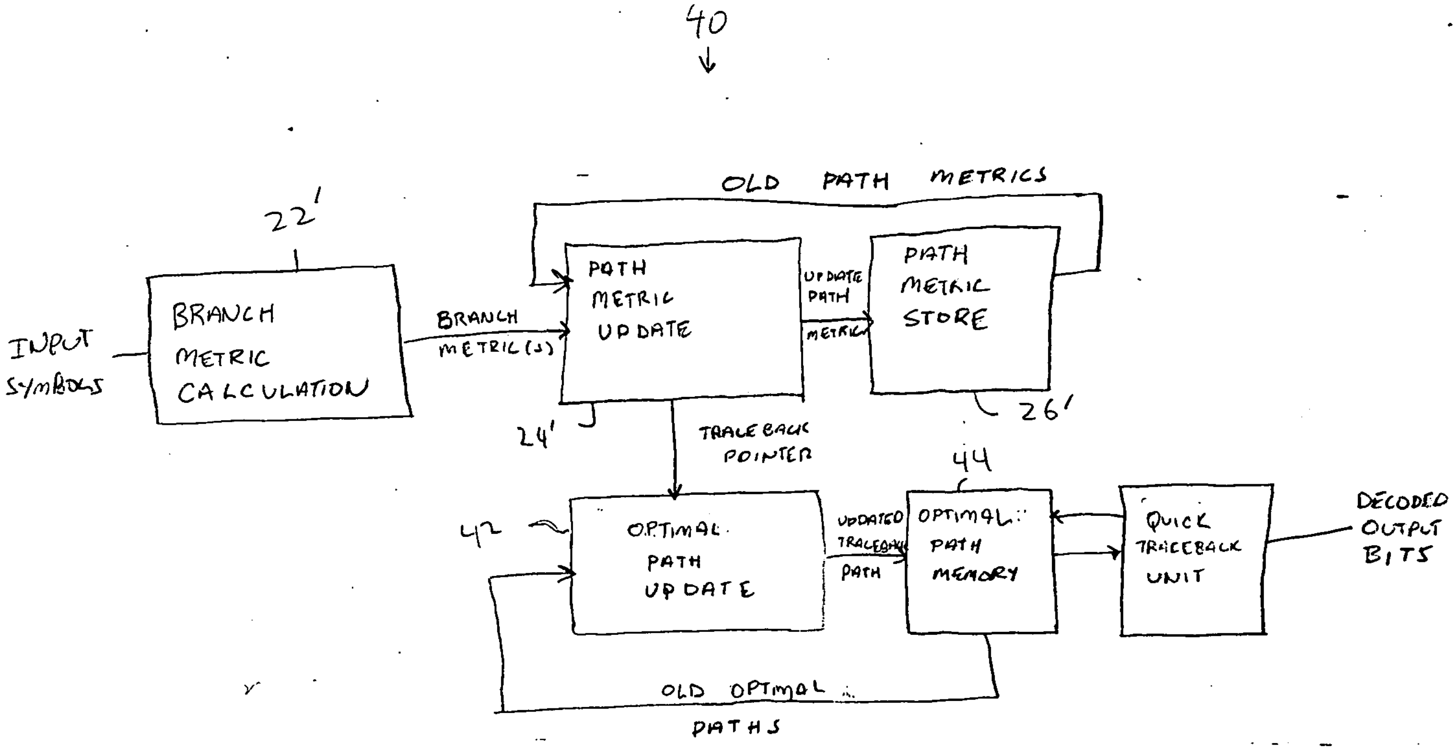

40
OLD PATH METRICS
22'
BRANCH METRIC CALCULATION
INPUT SYMBOLS
BRANCH METRIC(S)
PATH METRIC UPDATE
UPDATE PATH METRIC
PATH METRIC STORE
24'
26'
TRACE BACK POINTER
44
42
OPTIMAL PATH UPDATE
UPDATED TRACEBACK PATH
OPTIMAL PATH MEMORY
QUICK TRACEBACK UNIT
DECODED OUTPUT BITS
OLD OPTIMAL PATHS

FIGURE 2

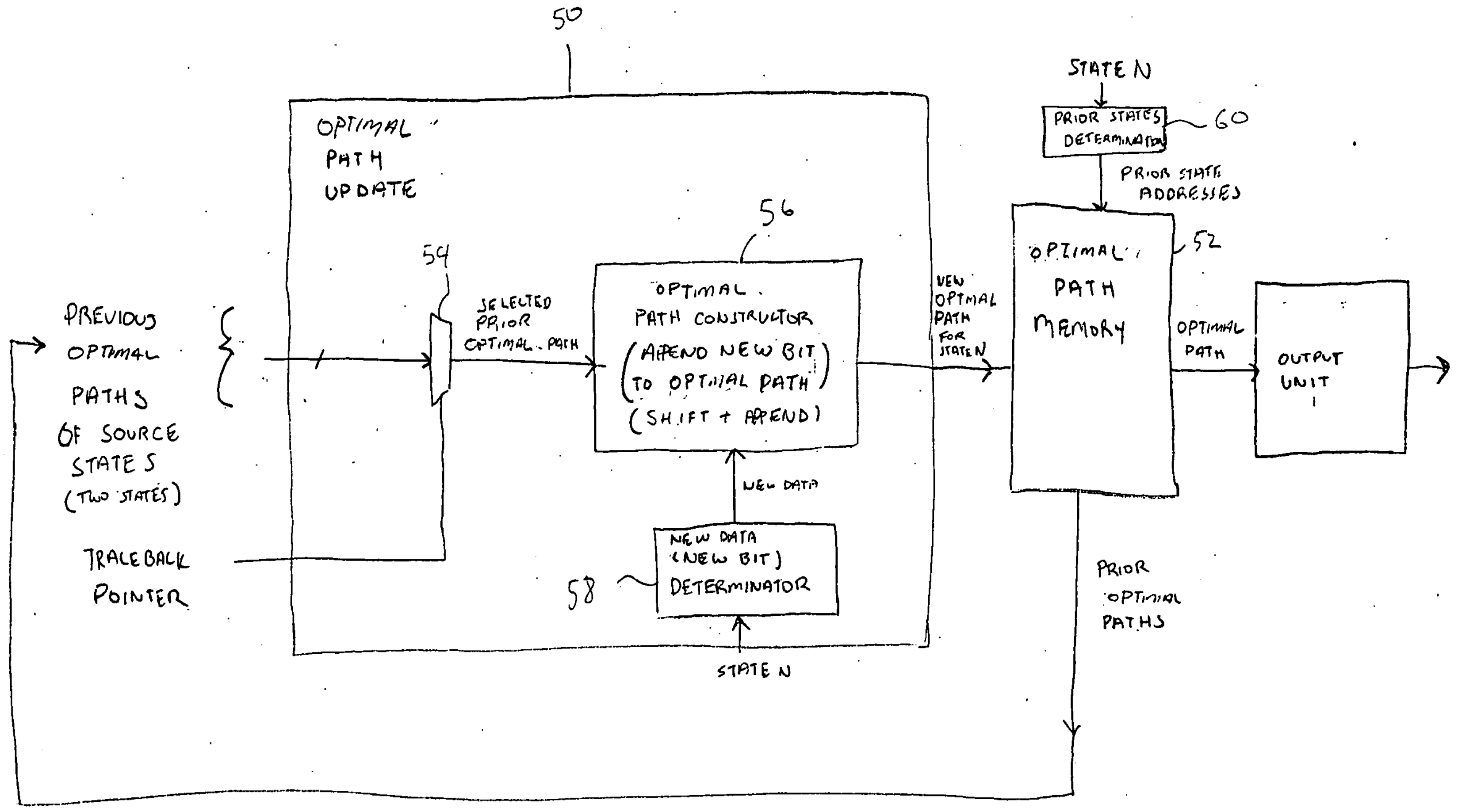

50
OPTIMAL PATH UPDATE
54
SELECTED PRIOR OPTIMAL PATH
56
OPTIMAL PATH CONSTRUCTOR (APPEND NEW BIT TO OPTIMAL PATH) (SHIFT + APPEND)
NEW DATA
58
NEW DATA (NEW BIT) DETERMINATOR
STATE N
PREVIOUS OPTIMAL PATHS OF SOURCE STATES (TWO STATES)
TRACEBACK POINTER
NEW OPTIMAL PATH FOR STATE N
STATE N
PRIOR STATES DETERMINATOR
60
PRIOR STATE ADDRESSES
52
OPTIMAL PATH MEMORY
OPTIMAL PATH
OUTPUT UNIT
PRIOR OPTIMAL PATHS

FIGURE 3

16-State Convolutional Encoder State Transition Graph

FOR RATE 1/2 CONVOLUTION CODE

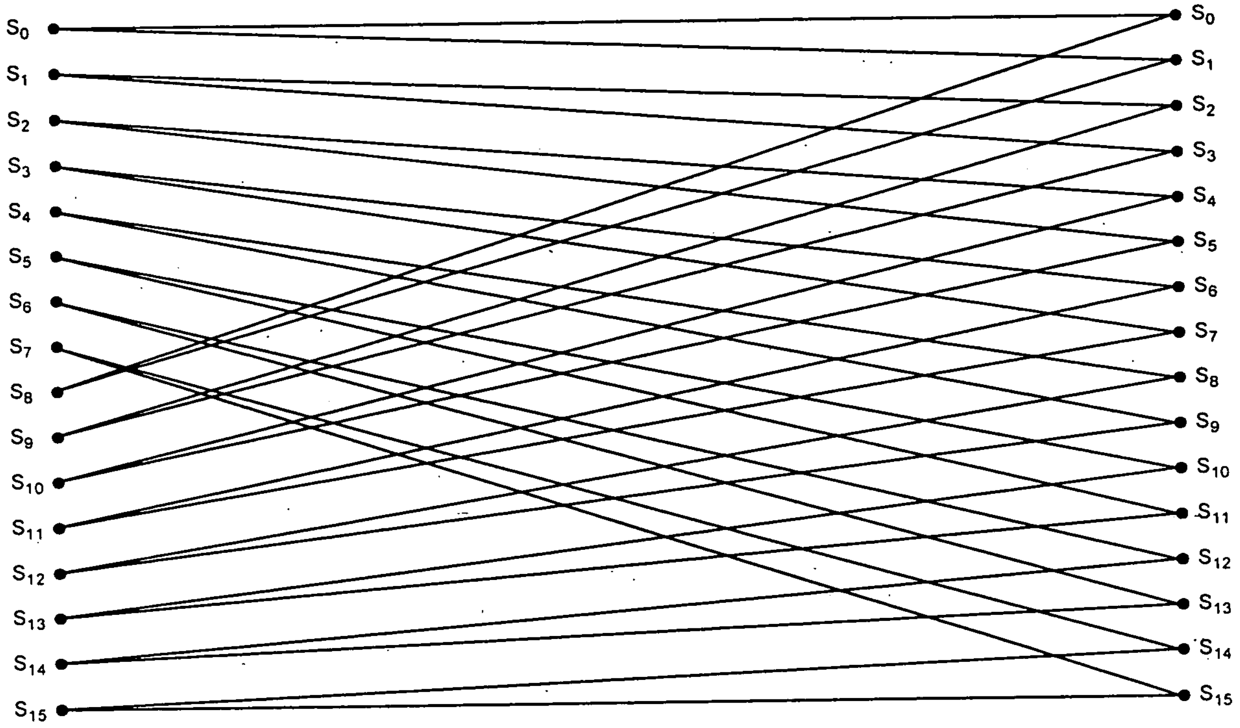


FIGURE 4

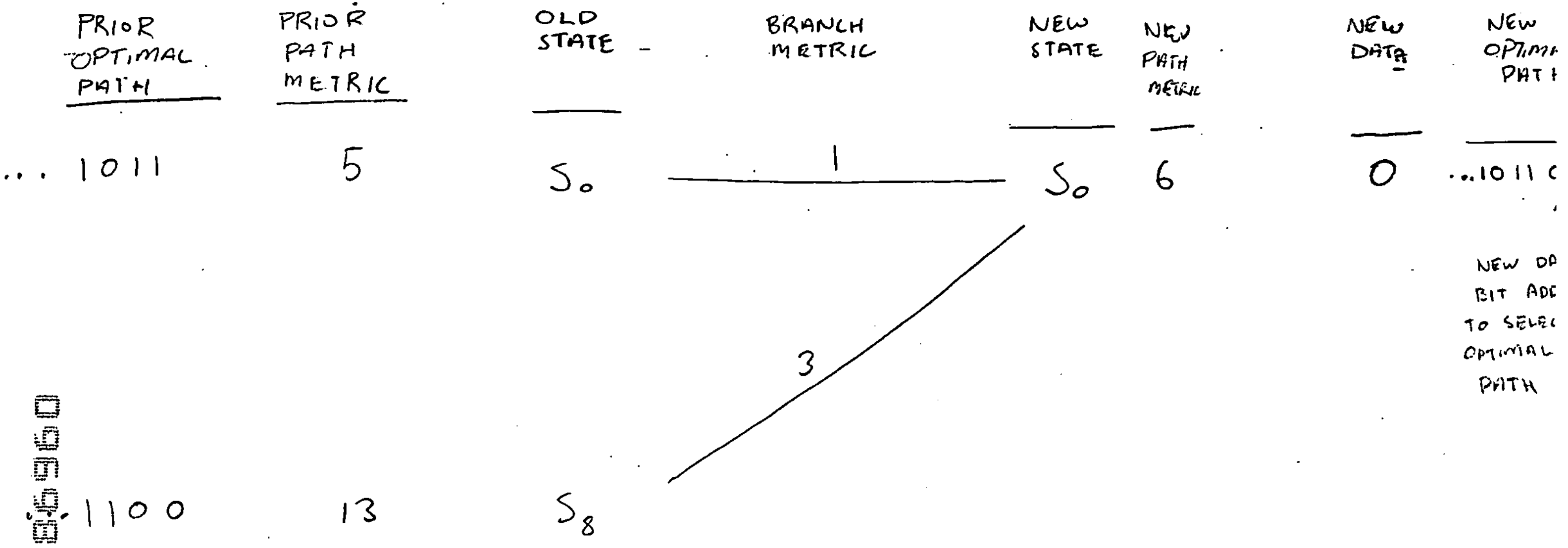

PRIOR OPTIMAL PATH
PRIOR PATH METRIC
OLD STATE
BRANCH METRIC
NEW STATE
NEW PATH METRIC
NEW DATA
NEW OPTIMA
PATH
... 1011
5
S_0
1
S_0
6
0
...1011 C
NEW DA
BIT ADD
TO SELEC
OPTIMAL
PATH
3
... 1100
13
S_8

FIGURE 5

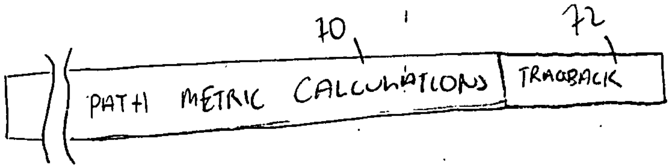


FIGURE 6A
(CONVENTIONAL)

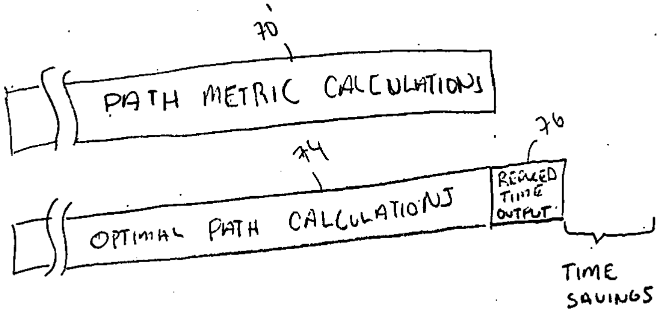


FIGURE 6B

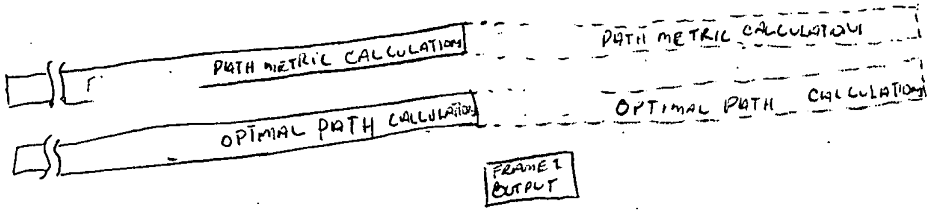


FIGURE 6C

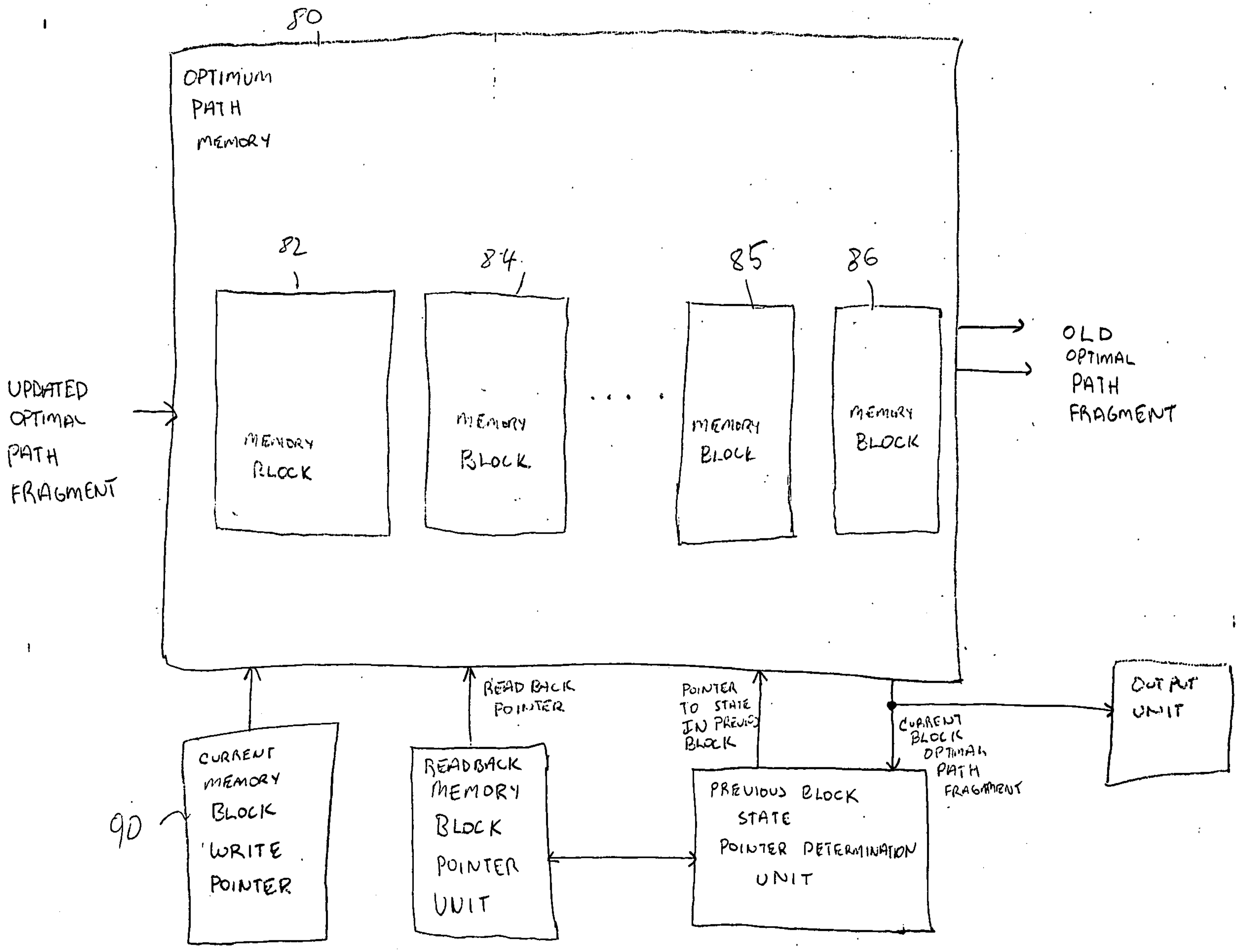

80
OPTIMUM PATH MEMORY
82
84
85
86
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
UPDATED OPTIMAL PATH FRAGMENT
OLD OPTIMAL PATH FRAGMENT
90
CURRENT MEMORY BLOCK WRITE POINTER
READBACK MEMORY BLOCK POINTER UNIT
READ BACK POINTER
PREVIOUS BLOCK STATE POINTER DETERMINATION UNIT
POINTER TO STATE IN PREVIOUS BLOCK
CURRENT BLOCK OPTIMAL PATH FRAGMENT
OUTPUT UNIT

FIGURE 7

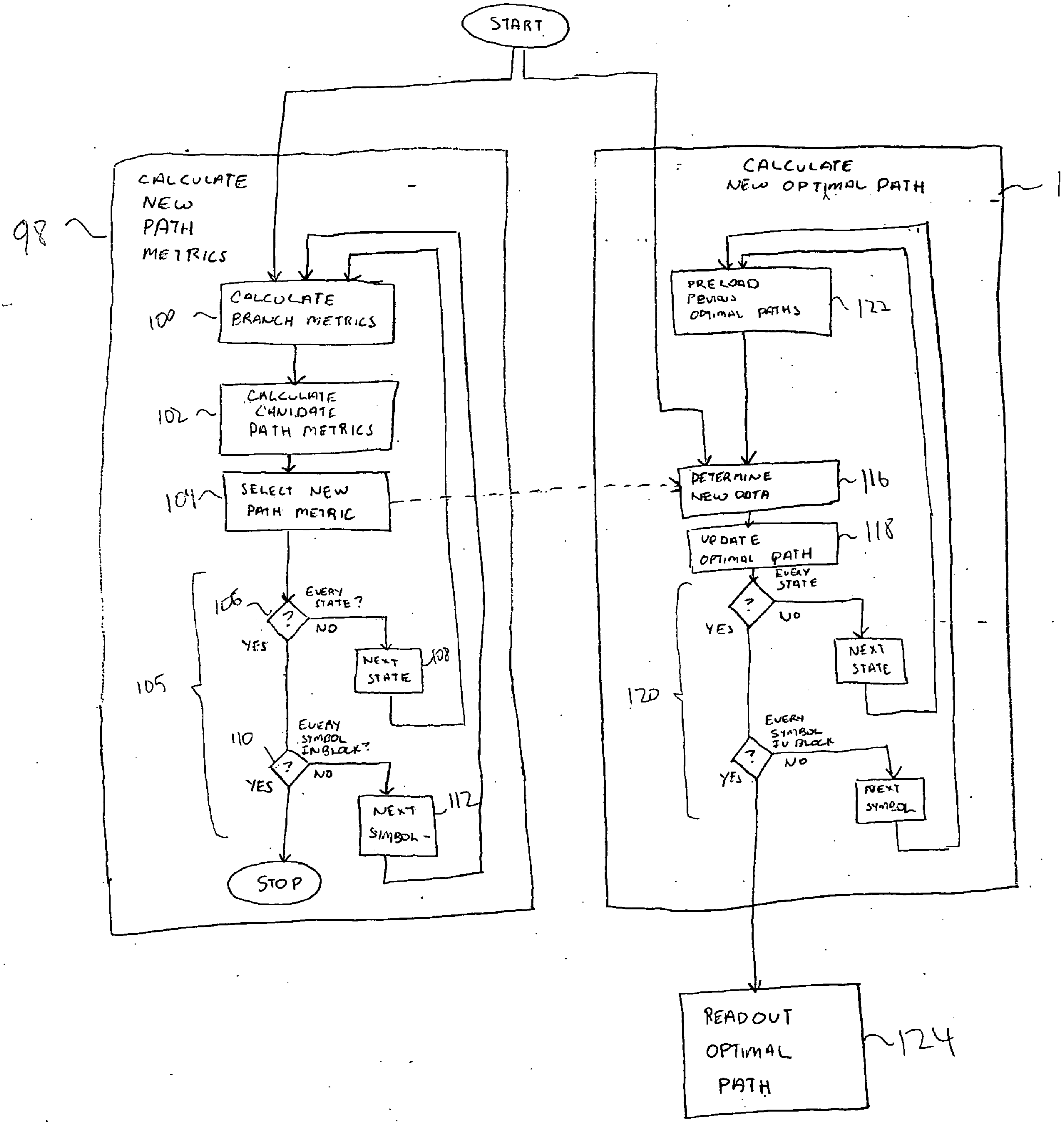

START
CALCULATE NEW PATH METRICS
98
CALCULATE BRANCH METRICS
100
CALCULATE CANIDATE PATH METRICS
102
SELECT NEW PATH METRIC
104
EVERY STATE ?
106
YES
NO
NEXT STATE
108
105
EVERY SYMBOL IN BLOCK ?
110
YES
NO
NEXT SYMBOL
112
STOP
CALCULATE NEW OPTIMAL PATH
114
PRELOAD PEVIOUS OPTIMAL PATHS
122
DETERMINE NEW DATA
116
UPDATE OPTIMAL PATH
118
EVERY STATE
?
YES
NO
NEXT STATE
120
EVERY SYMBOL IN BLOCK
?
YES
NO
NEXT SYMBOL
READOUT OPTIMAL PATH
124

FIGURE 8

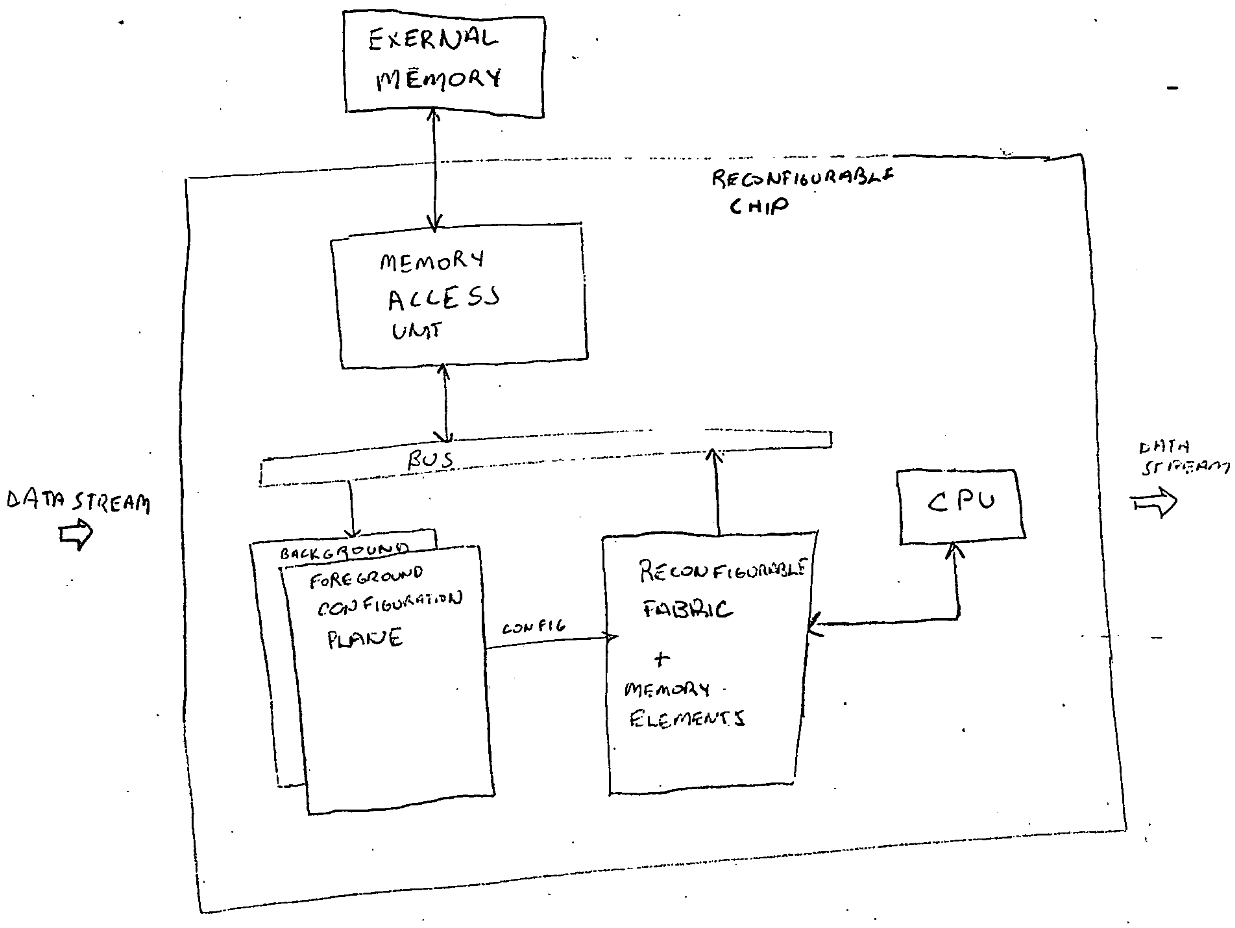

EXERNAL MEMORY
RECONFIGURABLE CHIP
MEMORY ACCESS UNIT
BUS
DATA STREAM
DATA STREAM
CPU
BACKGROUND
FOREGROUND CONFIGURATION PLANE
CONFIG
RECONFIGURABLE FABRIC + MEMORY ELEMENTS

FIGURE 9

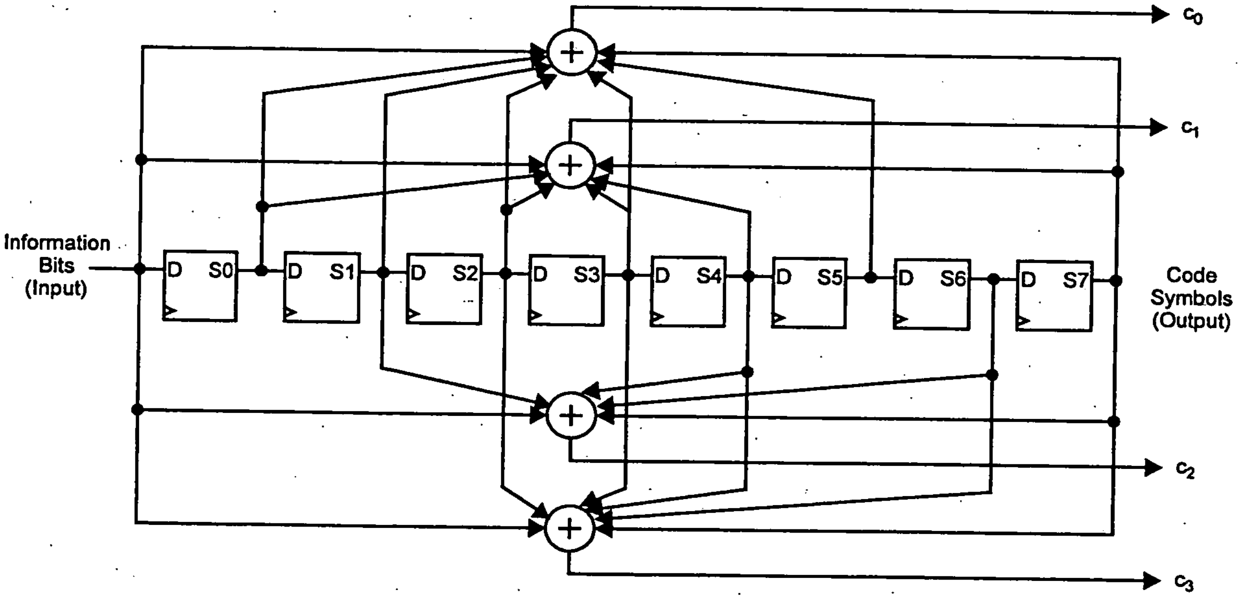

c0
c1
Information
Bits
(Input)
D S0
D S1
D S2
D S3
D S4
D S5
D S6
D S7
Code
Symbols
(Output)
c2
c3

FIGURE 10

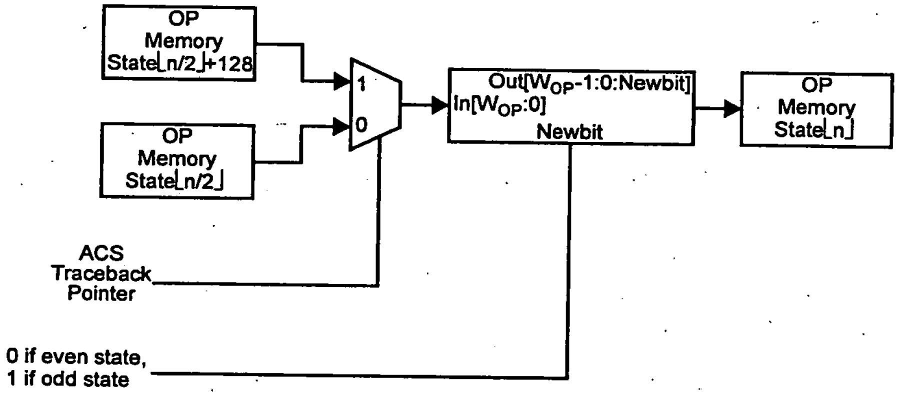

OP
Memory
State⌊n/2⌋+128
OP
Memory
State⌊n/2⌋
1
0
Out[W_{OP}-1:0:Newbit]
In[W_{OP}:0]
Newbit
OP
Memory
State⌊n⌋
ACS
Traceback
Pointer
0 if even state,
1 if odd state

FIGURE 11

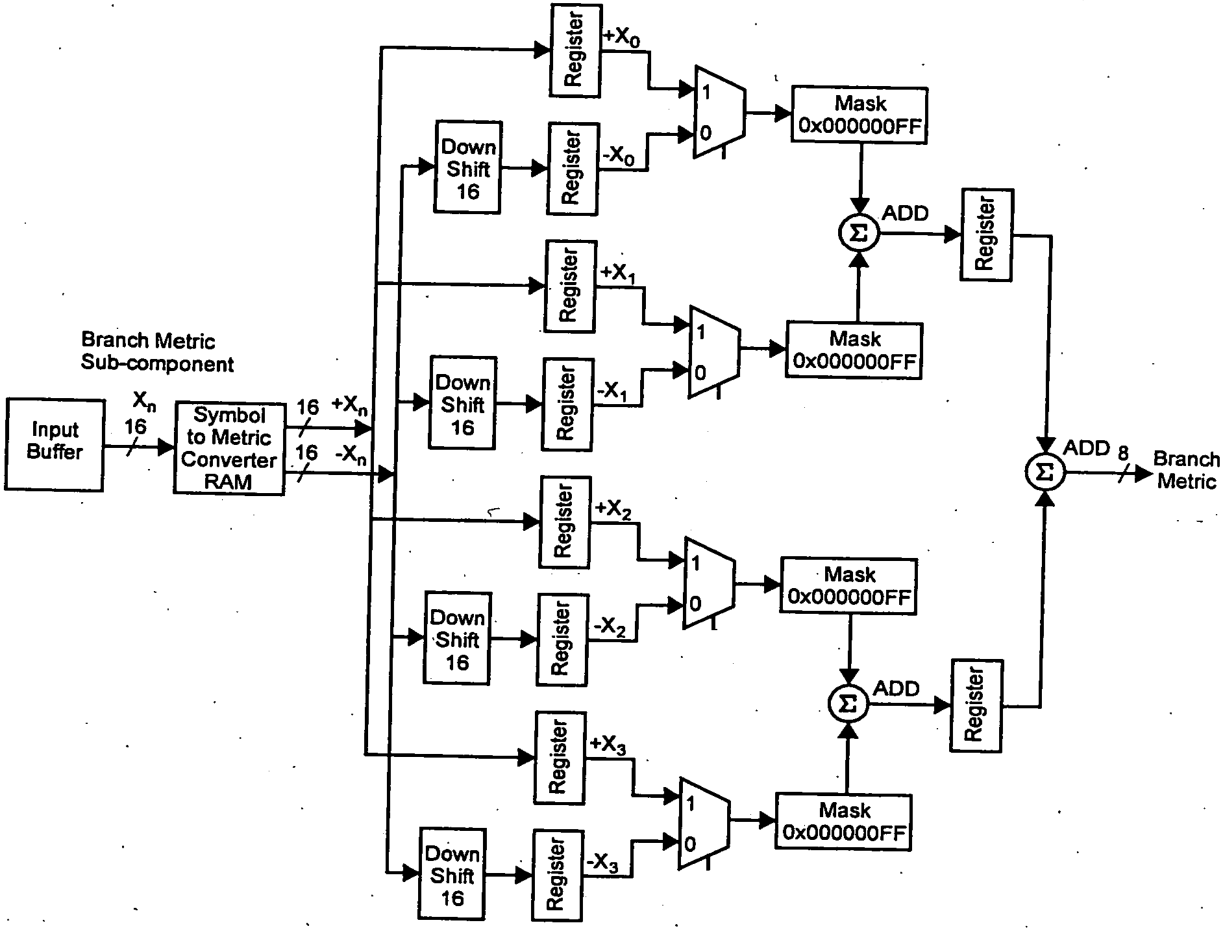

Branch Metric
Sub-component
Input Buffer
X_n
16
Symbol to Metric Converter RAM
16
$+X_n$
16
$-X_n$
Register
$+X_0$
Down Shift 16
Register
$-X_0$
1
0
Mask 0x000000FF
ADD
Register
Register
$+X_1$
Down Shift 16
Register
$-X_1$
1
0
Mask 0x000000FF
ADD
8
Branch Metric
Register
$+X_2$
Down Shift 16
Register
$-X_2$
1
0
Mask 0x000000FF
ADD
Register
Register
$+X_3$
Down Shift 16
Register
$-X_3$
1
0
Mask 0x000000FF

FIGURE 12

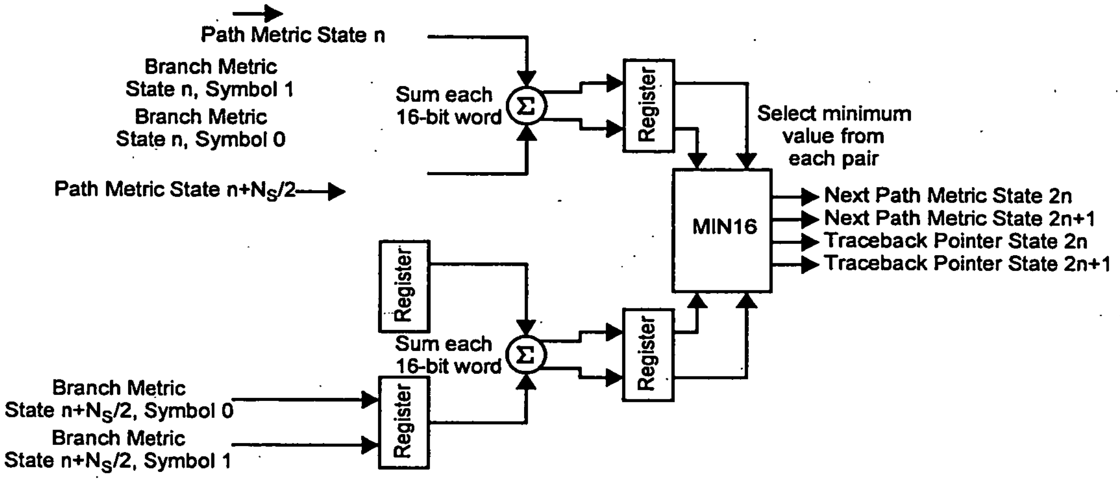

Path Metric State n
Branch Metric State n, Symbol 1
Branch Metric State n, Symbol 0
Path Metric State n+N_S/2
Sum each 16-bit word
Σ
Register
Select minimum value from each pair
MIN16
Next Path Metric State 2n
Next Path Metric State 2n+1
Traceback Pointer State 2n
Traceback Pointer State 2n+1
Register
Sum each 16-bit word
Σ
Register
Register
Branch Metric State n+N_S/2, Symbol 0
Branch Metric State n+N_S/2, Symbol 1

FIGURE 13

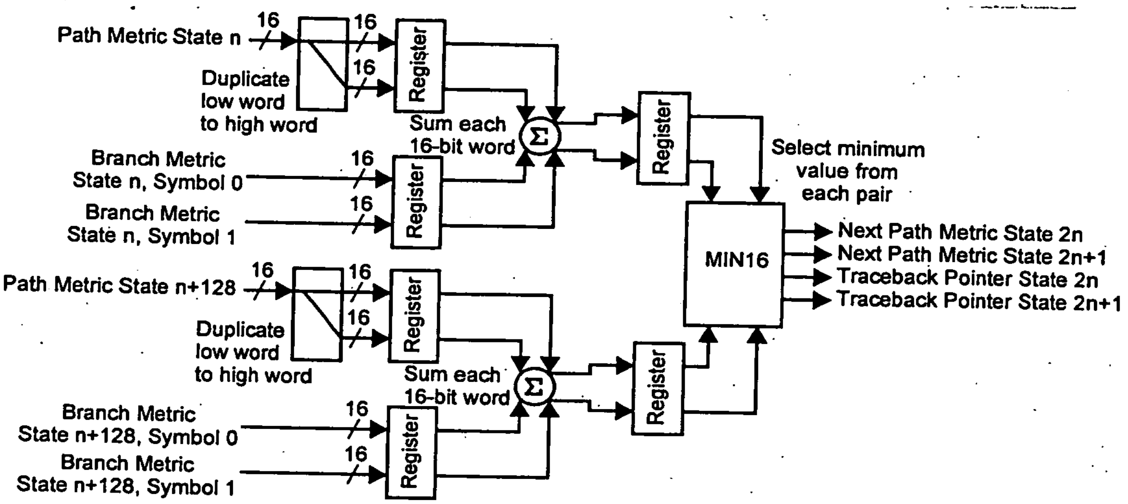
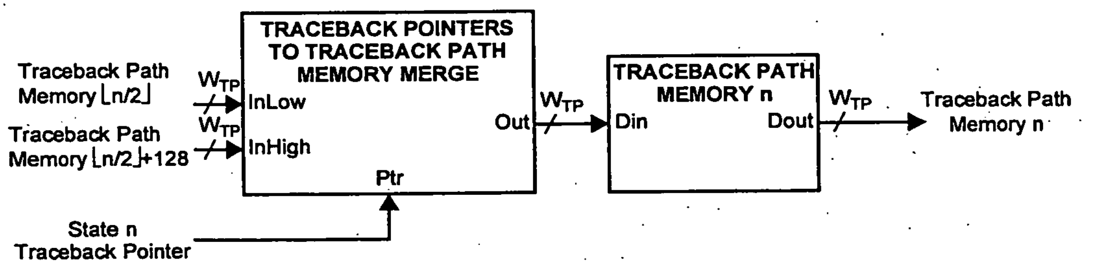


FIGURE 14



TRACEBACK PATH MEMORY SELECT TRUTH TABLE

Sel	Out
0	Ptr:(TP Mem ⌊n/2⌋)[14:0]
1	Ptr:(TP Mem ⌊n/2⌋+128)[14:0]

FIGURE 15

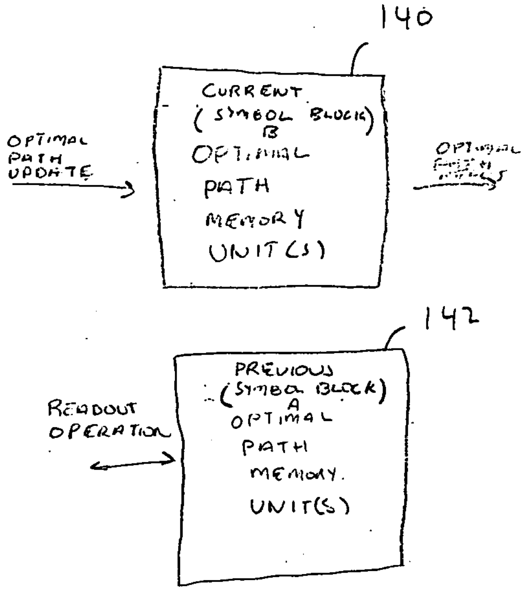


FIGURE 16A

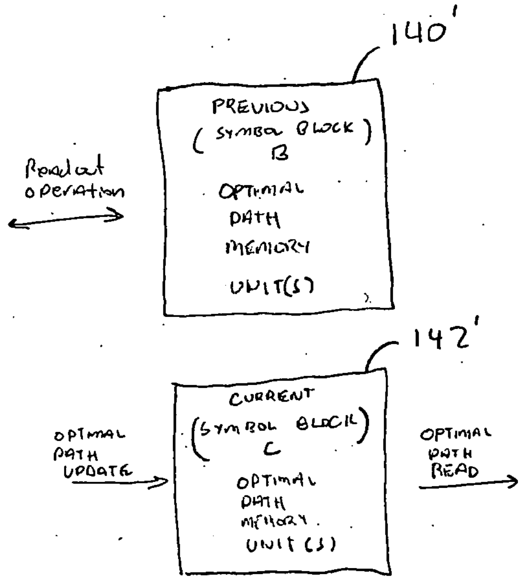


FIGURE 16 B